REMARKS

The added claims more completely claim the subject matter disclosed in the patent. Support for the added claims is found in the description of the first, fourth, and sixth embodiments and the description in column 13, lines 62-65. The amendments to claims 5-7 and 9 correct obvious informalities.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HATAKENAKA et al.

Application No.:	Unassigned	Art Unit:	Unassigned
Filed:	June 4, 2001	Examiner:	Unassigned
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE COMPRISING SYNCHRONOUS DRAM CORE AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND METHOD OF TESTING THE SYNCHRONOUS DRAM CORE		

SPECIFICATION, CLAIMS AND ABSTRACT AS PRELIMINARILY AMENDED

Amendments to the existing claims:

5. (Amended) [A]The semiconductor integrated circuit device according to claim 1 further comprising:

external input terminal means for transmitting external control signals for said synchronous dynamic random access memory;

synchronizing means for receiving the external control signals from said external input terminal means and outputting external control signals synchronized with a clock signal of said semiconductor integrated circuit; [and]

a command decoder for decoding the external control signals received from said synchronizing means into a first group of internal control signals for controlling said core unit of said synchronous dynamic random access memory; and

select means for supplying internal control signals to said core unit of said synchronous dynamic random access memory, the internal control signals being obtained by selecting either the first group of internal control signals received from said command decoder or a second group of internal control signals received from said synchronous dynamic random access memory control circuit, wherein said select means has a first mode selecting the first group of signals received from said command decoder and a second mode selecting the second group of signals received from said synchronous dynamic random access memory control circuit.

6. (Amended) The semiconductor integrated circuit device according to claim 1 further comprising:

external input terminal means for transmitting external control signals for said synchronous dynamic random access memory;

a command decoder for decoding the external control signals received from said external input terminal means into internal control signals for controlling said core unit of said synchronous dynamic [internal control signals] random access memory;

[a] synchronizing means receiving the internal control signals from said command decoder for outputting a first group of internal control signals synchronized with a clock signal of said semiconductor integrated circuit; and

select means for supplying the internal control signals to said core unit of said synchronous dynamic random access memory, the internal control signals being obtained by selecting either the first group of internal control signals received from said synchronizing means or a second group of internal control signals received from said synchronous dynamic random access memory control circuit, wherein said select means has a first mode selecting the first signals received from said synchronizing means and a second mode selecting the second signals received from said synchronous dynamic random access memory control circuit.

7. (Amended) A method for testing a semiconductor integrated circuit device, said test method including [the steps of comprising]:

a logic circuit and a synchronous dynamic random access memory including a core unit, said logic circuit and said synchronous dynamic random access memory being integrated into a single semiconductor chip; and

providing external test signals through external input terminal means to a selector;

providing internal control signals from a synchronous dynamic random access memory control circuit to a selector; and

selecting said external test signals from said external input terminal means, using said selector, for providing the selected signals to a core unit of said synchronous dynamic random access memory for testing.

9. (Amended) The method for testing a semiconductor integrated circuit device according to claim 7, wherein the external test signals are external control signals for said core unit of said synchronous dynamic random access memory, and [is] are decoded by a decoder to be the internal control signals provided to said selector.

Add the following claims:

10. (New) A semiconductor integrated circuit device comprising:

a logic circuit and a random access memory with a command decode system including a core unit, said logic circuit and said random access memory with a command decode system being integrated into a single semiconductor chip; and

a random access memory with a command decode system receiving external control signals for said random access memory with a command decode system from said logic circuit, and outputting signals to said core unit of said random access memory with a command decode system wherein the output signals from said random access memory with a command decode system are internal control signals for controlling said core unit of said random access memory with a command decode system.

11. (New) The semiconductor integrated circuit device according to claim 10 further comprising:

external input terminal means for transmitting a first group of internal control signals for said random access memory with a command decode system; and

select means for supplying internal control signals to said core unit of said random access memory with a command decode system, said internal control signals being obtained by selecting either the first group of internal control signals received from said external input terminal means or a second group of internal control signals received from said random access memory with a command decode system, wherein said select means has a first mode selecting the first group of signals received from said external input terminals for testing said semiconductor integrated circuit device with the first group of signals, and a second mode selecting the second group of signals received from said random access memory with a command decode system.

12. (New) The semiconductor integrated circuit device according to claim 10 further comprising:

external input terminal means for transmitting internal control signals for said random access memory with a command decode system;

synchronizing means for receiving the internal control signals from said external input terminal means and outputting a first group of internal control signals synchronized with a clock signal of said semiconductor integrated circuit; and

select means for supplying internal control signals to said core unit of said random access memory with a command decode system, said internal control signals being obtained by selecting either the first group of internal control signals received from said synchronizing means or a second group of internal control signals received from said random access memory with a command decode system, wherein said select means has a first mode selecting the first group of signals received from said synchronizing means, and a second mode selecting the second group of signals received from said random access memory with a command decode system.

13. (New) The semiconductor integrated circuit device according to claim 10 further comprising:

external input terminal means for transmitting external control signals for said random access memory with a command decode system;

a command decoder for decoding the external control signals received from said external input terminal means into a first group of internal control signals for controlling said core unit of said random access memory with a command decode system; and

select means for supplying internal control signals to said core unit of said random access memory with a command decode system, the internal control signals being obtained by selecting either the first group of internal control signals received from said command decoder or a second group of internal control signals received from said random access memory with a command decode system, wherein said select means has a first mode selecting the first group of signals received from said command decoder, and a second mode for selecting the second group of signals received from said random access memory with a command decode system.

14. (New) The semiconductor integrated circuit device according to claim 10 further comprising:

external input terminal means for transmitting external control signals for said random access memory with a command decode system;

synchronizing means for receiving the external control signals from said external input terminal means and outputting external control signals synchronized with a clock signal of said semiconductor integrated circuit;

a command decoder for decoding the external control signals received from said synchronizing means into a first group of internal control signals for controlling said core unit of said random access memory with a command decode system; and

select means for supplying internal control signals to said core unit of said random access memory with a command decode system, the internal control signals being obtained by selecting either the first group of internal control signals received from said command decoder or a second group of internal control signals received from said random access memory with a command decode system, wherein said select means has a

first mode selecting the first group of signals received from said command decoder and a second mode selecting the second group of signals received from said random access memory with a command decode system.

15. (New) The semiconductor integrated circuit device according to claim 10 further comprising:

external input terminal means for transmitting external control signals for said random access memory with a command decode system;

a command decoder for decoding the external control signals received from said external input terminal means into internal control signals for controlling said core unit of said random access memory with a command decode system;

synchronizing means receiving the internal control signals from said command decoder for outputting a first group of internal control signals synchronized with a clock signal of said semiconductor integrated circuit; and

select means for supplying the internal control signals to said core unit of said random access memory with a command decode system, the internal control signals being obtained by selecting either the first group of internal control signals received from said synchronizing means or a second group of internal control signals received from said random access memory with a command decode system, wherein said select means has a first mode selecting the first signals received from said synchronizing means and a second mode selecting the second signals received from said random access memory with a command decode system.

16. (New) A method for testing a semiconductor integrated circuit device, said test method including:

a logic circuit and a random access memory with a command decode system including a core unit, said logic circuit and said random access memory with a command decode system being integrated into a single semiconductor chip; and

providing external test signals through external input terminal means to a selector;

providing internal control signals from a random access memory with a command decode system to a selector; and

selecting said external test signals from said external input terminal means, using said selector, for providing the selected signals to a core unit of said random access memory with a command decode system for testing.

17. (New) The method for testing a semiconductor integrated circuit device according to claim 16, wherein the external test signals are internal control signals for testing said core unit of said random access memory with a command decode system.

18. (New) The method for testing a semiconductor integrated circuit device according to claim 16, wherein the external test signals are external control signals for said core unit of said random access memory with a command decode system, and are decoded by a decoder to be the internal control signals provided to said selector.